Chip-to-Module Interconnections Using "Sea of Leads" Technology

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Abstract

The drive toward higher density and higher performance in integrated circuits creates a need to keep interconnects short and eliminate layers of packaging. In this article, we propose a novel, ultrahigh-density (exceeding 10^4 leads per cm^2), compliant, wafer-level, input/output interconnection technology called "sea of leads" as a key enabling technology for future high-performance microsystems. The mechanical compliance is addressed through slippery leads (leads released from the surface) and embedded air gaps. The ability to fabricate embedded air gaps has enabled the integration of optical interconnects with high index-of-refraction mismatches between the core and cladding.

Keywords: *elastic properties, electronic materials, interconnections, microelectronics packaging and integration, optical properties, semiconductors.*

Introduction

Silicon technology has exponentially increased in performance and productivity over the past four decades. Moore's law, which quantifies this rate of increase, asserts that the density of transistors doubles about every 18 months. The simultaneous improvement in density of transistors and performance is a direct result of shrinking the size of the transistor. Table I lists several projections taken from the International Technology Roadmap for Semiconductors (ITRS).[1–3] The smaller transistor size (technology generation) results in shorter switching delays, lower switching energies, and higher clock frequencies. However, wires do not improve with shrinking dimensions. In fact, the interconnect response time is a very significant problem, along with the processing issues resulting from increased wiring levels and longer wire lengths. The number of chip input/output (I/O) interconnects increases with chip functionality. This puts an added burden on performance at the substrate or board level (i.e., the next level of packaging). Cost-effective packages are required in order to maintain the present trends in systems costs. No packaging technology has yet been able to satisfy simultaneously these performance and cost requirements.

Improvement in electrical performance and reduction in the cost of packages both lead to a reduction in the number of packaging levels. Chip-scale packaging and direct chip-on-board technologies (i.e., chips mounted directly to the circuit board with no intervening layers of packaging) are clear trends in that direction. In this article, we discuss the need for wafer-level packaging (WLP), performed while the die are in wafer form, that addresses the need for mechanical compliance.

Compliance is critical to accommodating the mechanical strains that result from thermal-expansion mismatches of parts as well as warpage and bending of components (chips and boards). In our WLP process, conventional chip manufacturing (front-end of the line and back-end of the line processes) is extended to include tail-end of the line processing. Front-end processing refers to the fabrication of transistors, while back-end processing refers to wafer metallization. Tail-end processing is used to fully package the individual die.

Conventionally, the final back-end wafer-level processing step is the fabrication of vias through a passivation layer to expose the pads on the die that serve as the interface between the die and the package. Each individual die, while still part of the wafer, then undergoes wafer-sorting to identify known good die (KGD), after which wafer singulation (cutting a wafer into individual die) is performed. The KGDs

Table I: Projections for 1.0-μm, 100-nm, and 35-nm Technology Generations.

	Technology Generation		
	1.0 μm	**100 nm**	**35 nm**
MOSFET[a] switching delay	~20 ps	~5 ps	~2.5 ps
Interconnect response time (L_{int} = 1 mm)[b]	~1 ps	~30 ps	~250 ps
MOSFET switching energy	~300 *f*J	~2 *f*J	~0.1 *f*J
Interconnect switching energy	~400 *f*J	~10 *f*J	~3 *f*J
Clock frequency	~30 MHz	~2–3.5 GHz	~3.6–13.5 GHz
Supply current	~2.5 A (V_{dd} = 5.0 V)[c]	~150 A (V_{dd} = 1.0 V)	~360 A (V_{dd} = 0.5 V)
Maximum number of wiring levels	3	8–9	10
Maximum total wire length per chip	100 m	~5000 m	…
Chip pad count	~200	~3000–4000	4000–4400

Source: *2001 International Technology Roadmap for Semiconductors.*[3]
[a] MOSFET = metal oxide semiconductor field-effect transistor.
[b] L_{int} = interconnect length.
[c] V_{dd} = power-supply voltage.

are then shipped to a packaging foundry, where they are individually placed in temporary packages for burn-in, an accelerated aging process performed at high voltage and temperature to weed out faulty units. The die that pass this test are then individually packaged and retested for functionality. In our WLP approach, following the final step in tail-end processing, all die are fully packaged and tested and are immediately ready for final system assembly after wafer singulation.

"Sea of Leads": Concept

"Sea of leads" (SoL) is a novel, ultrahigh-density (exceeding 10^4 leads per cm^2), compliant wafer-level I/O interconnection technology proposed as a key enabler of future high-performance microsystems.[1,2,4,5] The overhead testing and temporary assembly steps in conventional packaging are reduced with the use of SoL because the die are tested in wafer form prior to singulation. Die that are identified as nonfunctional are never packaged, which saves time and money. In the compliant wafer-level packaging (CWLP) scheme, "compliant" meaning that the leads are elastically deformable in all three directions, a series of massively parallel monolithic processing steps are used to provide the die with x–y–z compliant leads, as depicted in Figure 1. Thus, this approach extends the economic benefits of wafer-level front-end and back-end processing to the batch fabrication of compliant, high-performance I/O interconnects and wafer-level testing.[4–7] Die with SoL I/O interconnects may be mounted on substrates with significantly higher coefficients of thermal expansion (CTEs) without the need for underfill (the addition of a polymer layer between chip and package), due to the compliant nature of the I/O interconnects. In addition, z-axis compliance allows reliable electrical contact to be attained between nonplanar wafer and probe-card surfaces during wafer-level testing and burn-in. Using these concepts, low-I/O-count CWLP with 256 I/O interconnects has been bonded and tested for reliability and has demonstrated the potential of surviving 1500 thermal cycles before failing in an air-to-air thermal chamber.[6,7]

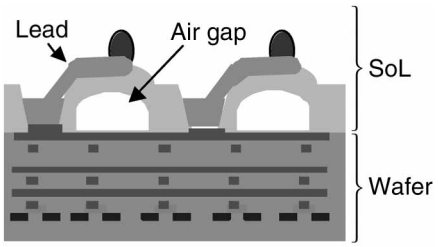

Figure 1. A schematic representation of a "sea of leads" (SoL) chip. Through a series of monolithic processing steps, die across a wafer are packaged with a compliant interposer and leads, enabling wafer-level testing and burn-in. In essence, SoL extends wafer-level batch processing of multilayer interconnect networks to include chip input/output leads.

"Sea of Leads": Fabrication

Through a series of wafer-level processing steps, compliant S-shaped metal leads are fabricated above a polymer film with highly compressible embedded air gaps, as shown in Figure 2. A schematic illustration of the fabrication process is illustrated in Figure 3. The first step in SoL fabrication is the application and patterning of the sacrificial polymer, with the patterned geometry ultimately being the shape of the air gap. The details of this polymer are covered later. Next, an overcoat polymer is deposited on the wafer to encapsulate the patterned sacrificial polymer. The wafer is then placed in a furnace, where the sacrificial polymer is thermally decomposed (with the gaseous products permeating through the overcoat) to form an air gap embedded within the overcoat polymer. Next, vias are fabricated in the overcoat polymer to expose the die pads and allow electrical interconnection to the chip.

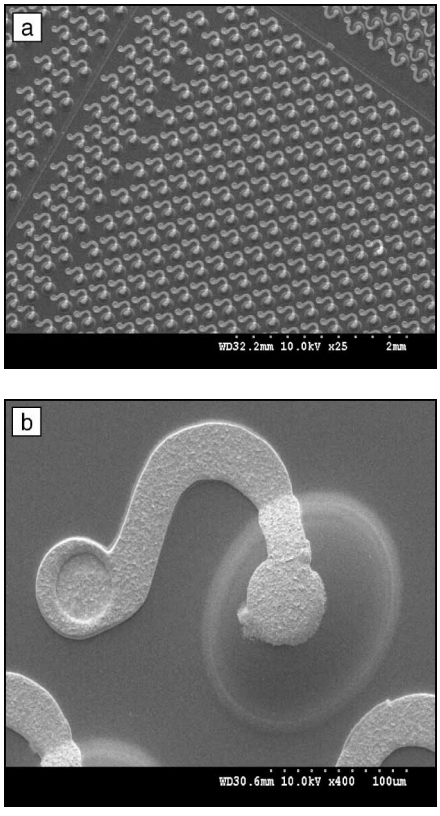

Figure 2. Scanning electron microscopy images of (a) an array and (b) a close-up view of S-shaped compliant metal leads fabricated above a polymer film embedded with highly compressible air gaps.

At this stage, two different methods are used to control the adhesion of the leads to the overcoat polymer. Since the leads are typically ~10 μm thick and must be resilient to oxidization, gold is an effective metallization. Thickness not only influences the lead's force-displacement behavior, but it also influences its electrical performance. In Method 1 (Figure 3), the adhesion of the lead to the overcoat polymer is controlled by seed-layer selection. For strong adhesion to the overcoat polymer, a Ti/Au seed layer is sputter-deposited, where the Ti functions as a glue layer between the Au and the overcoat polymer. For poor adhesion (slippery leads), Au alone can be sputter-deposited on the wafer. Poor adhesion enhances the compliance of the leads. However, if the die pads are copper, as they are in the wafers described in this article, adhesion between the Cu pad and the Au seed layer is decreased without the Ti layer. As a result, in order to anchor the leads at the die pad end and leave the remainder of the lead free to move, electroless nickel can be plated on the Cu die pads as an adhesion promoter and diffusion barrier before the sputtering of the Au seed layer. Thus, the leads plated on the seed layer have good adhesion to the die pads, but adhere poorly to the overcoat polymer, so the leads will move easily if a force is applied.

The second method (Method 2 in Figure 3) of fabricating slippery leads is to plate the Au leads on a seed layer that is selectively etched away when the leads are ready to be released from the surface. This fabrication method was demonstrated by plating Au leads on a Ti/Cu seed layer. Following the fabrication of the leads, solder bumps are fabricated on the ends of the leads. Following bump fabrication, the Cu seed layer is first selectively etched away with a dilute nitric acid solution, and the Ti seed layer is etched next using buffered oxide etchant. This fabrication method, which uses selective seed-layer etching, is easier to implement because the leads only become slippery once the seed layer is selectively etched.

Slippery leads fabricated using Method 1 are shown in Figure 4. The lead on the left was observed to move easily in the

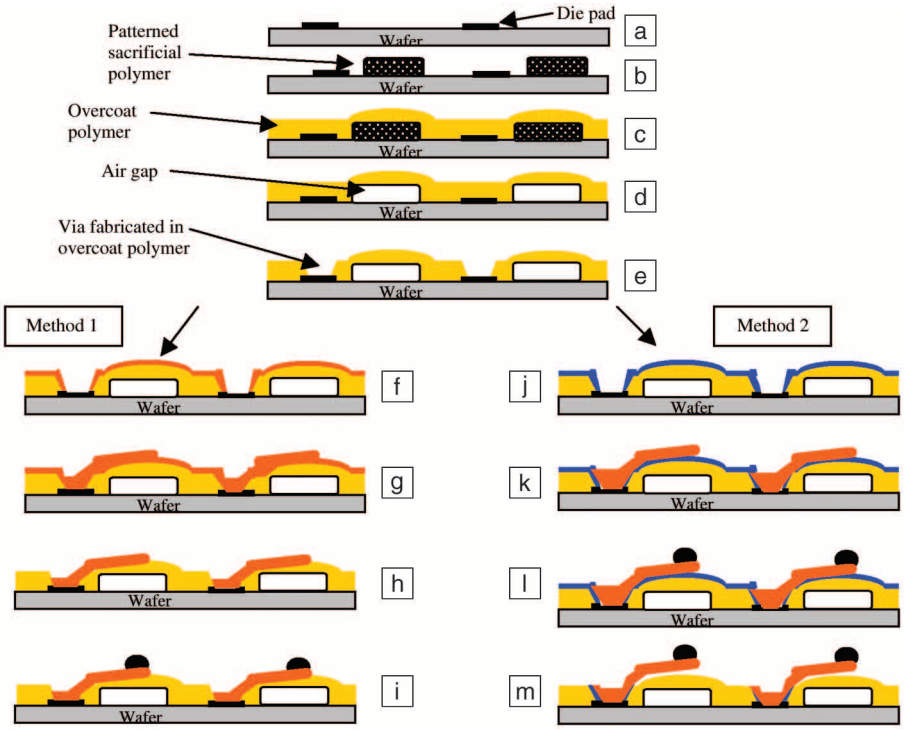

Figure 3. SoL fabrication process.[4] (a) Back-end-of-line processing is complete: die pads exposed through passivation. (b) Deposition and patterning of sacrificial material. (c) Application of overcoat polymer. (d) Sacrificial material decomposed to form air gaps. (e) Via fabrication in overcoat polymer to expose die pads. The wafer at this stage is ready for lead fabrication. Method 1: (f) Au seed layer is deposited, (g) Au leads are electroplated, (h) Au seed layer is etched away, and (i) solder bumps are fabricated on the leads. Method 2: (j) Ti/Cu seed layer is deposited, (k) Au leads are electroplated, (l) solder bumps are fabricated, and (m) seed layer is selectively etched away to release the leads from the polymer surface. The typical thickness of the Ti/Cu seed layer is 300 Å Ti/2000 Å Cu.

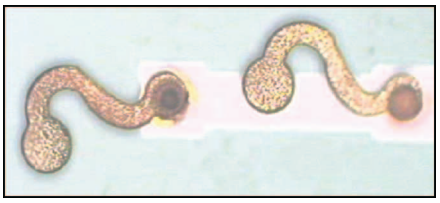

Figure 4. Micrograph showing slippery leads fabricated using Method 1 described in Figure 3 (i.e., using an Au seed layer). The lead on the left has moved by approximately 70 μm after the application of a lateral force.

x–y plane due to poor adhesion. Similar behavior was observed for the slippery leads fabricated using Method 2. SoL chips fabricated by these methods have an I/O density of 1000/cm^2. However, these processes can be extended to chips with much higher I/O density: 12,000/cm^2 leads have been demonstrated.[4,5]

The out-of-plane compliance for SoL interconnection technology is of particular interest here because it can be used in many applications, including probe cards (i.e., components used to electrically contact chips during testing) for wafer-level testing and burn-in.[8] The method of air-gap fabrication, patterning, encapsulation, and thermal decomposition of sacrificial polymers is unique because it allows complete control over air-gap geometry, and it also allows the formation of fully enclosed air-gap structures with no fill holes. In addition to sacrificial polymers patterned by reactive ion etching (RIE), the film can also be photochemically patterned.[9–11] Following encapsulation of the patterned sacrificial polymer with dielectric, the composite structure is heated to the decomposition temperature of the sacrificial polymer. The sacrificial polymer decomposes into volatile products that permeate through the encapsulating material and leave behind minimal solid residue. Embedded air gaps have been formed at a variety of temperatures using polymers such as Promerus LLC's Unity400 (decomposition temperature T_d = 400°C) and Unity200 (T_d = 200°C), in a variety of encapsulating low-κ materials, including plasma-enhanced chemical vapor deposition (PECVD) silicon dioxide and silicon nitride, polyimide, epoxy, Avatrel dielectric polymer, and benzocyclobutene. Air-gap sizes range from 0.25 μm to 1 cm in width and 500 nm to 50 μm in height. The sacrificial polymer is chosen so that the encapsulating material can be fully cured below the T_d of the sacrificial material. In addition, the thermal and mechanical properties and permeability of the overcoat material, and the rate of decomposition of the sacrificial material, can affect the final air-gap shape in the vertical direction. If the decomposition rate is high and the overcoat is flexible or can flow, a net pressure will build inside the air gap and the resultant gap will become dome-shaped.

For SoL I/O interconnection in particular, air gaps are used for out-of-plane (z axis) mechanical performance. The combination of the in-plane (x–y axis) flexible metal interconnect with an out-of-plane (z axis) compliant air gap creates an interconnect structure capable of moving in three directions. Through mechanical testing and modeling, the effects of air-gap geometry, encapsulating material thickness, and properties on z-axis compliance have been investigated. Depending on the level of compliance needed, the necessary air-gap shape and size can be predicted. For example, square air-gap structures, 190 μm × 190 μm and 30 μm tall, encapsulated in a polyimide with an elastic modulus of 5 GPa have shown z-axis compliance in the range of 1–2 mm/N and displacements of up to 30 μm. The use of a thin, low-modulus overcoat material results in the most flexible structures.

Optical I/Os

Some of the limitations of metallic electrical interconnects and I/Os can be overcome by the use of optical interconnects. Polymer waveguides hold tremendous potential for optical interconnection within applications such as gigascale fiber-to-the-chip (wherein data is supplied to the chip through optical fibers) and optical-clock distribution (making internal clock signals available to all parts of the system), as they offer process compatibility with existing microelectronics technology, low time-of-flight propagation delay, and the ability to integrate high-efficiency volume-grating couplers.

A volume grating is a passive diffractive optics device where the lines of refractive-index modulation responsible for light diffraction are contained within the volume of the material. Two structures exist for volume-grating couplers (depicted in

Figure 5).[12,13] The performance of each structure can be equivalent, depending on the optimization of design parameters.[12,14] For the grating-atop-the-waveguide structure shown in Figure 5a, the primary constraint imposed on a candidate waveguide core material by process compatibility is adhesion between the grating and waveguide layers. In terms of constraints imposed by performance, the core refractive index should be as close to that of the grating material as possible to allow for strong evanescent interaction between the supported mode and the grating region. For the grating-within-the-waveguide structure shown in Figure 5b, a material suitable for both the propagation of optical power and definition of volume-grating structures is essential. Such a material must be optically transparent and exhibit high resolution for defining submicron grating periods, high internal refractive-index modulation (here, a result of monomer diffusion mechanisms induced by UV exposure), and minimal material shrinkage upon thermal cure.

To date, optical waveguides have been fabricated within SoL WLP such that a buried air-gap region surrounds the waveguide core.[15] The waveguides can function within either grating-atop-the-waveguide or grating-within-the-waveguide structures. In the case of grating-within-the-waveguide volume gratings, the waveguides serve as the lower cladding region upon which the waveguide core layer resides. The lower cladding layer, constructed from an epoxy siloxane oligomer that uses mesitylene as the solvent,[16] has been investigated as a means of providing adhesion between the grating core region and fused-silica and SiO_2 substrates. The lower cladding material exhibits a refractive index in the range of 1.46–1.54 at a 632-nm optical wavelength, depending on composition. Propagation losses are dominated by scattering at the channel side walls due to use of RIE patterning, as well as scattering generated at the SiO_2/polymer interface.

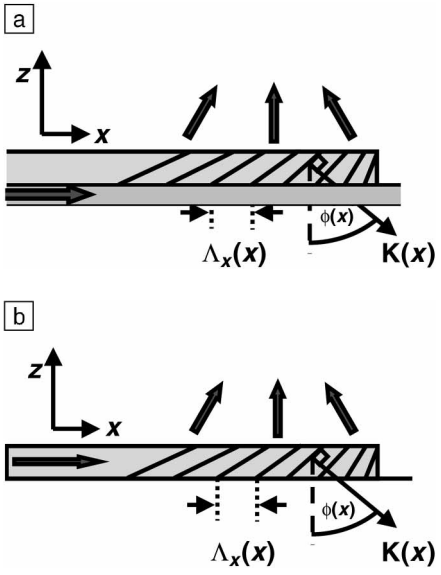

*Figure 5. (a) Grating-atop-the-waveguide volume-grating coupler. $\Lambda_x(x)$, $\phi(x)$, and **K**(x) are the grating period, slant angle, and grating vector, respectively.[12] (b) Grating-within-the-waveguide volume-grating coupler.[13]*

Volume-grating couplers were constructed using a laminate photopolymer material (Omnidex HRF600 from Dupont). To define a grating, the photopolymer is subject to UV (365 nm) radiation in the form of a fixed-intensity pattern with a predetermined period (~0.3 μm) and slant angle (~45°). This intensity pattern is created using an interferometric recording setup.

One method of defining either type of volume-grating coupler is as follows. The volume grating is first defined by exposing a stand-alone laminate sheet of photopolymer. During grating exposure, a prism and index-matching oil are used to couple light into the grating region at the angles of incidence required by the desired grating vector. Oil removal after exposure is achieved by rinsing the sample in isopropyl alcohol. After N_2 drying, the sample is then laminated onto a layer of epoxy, where the epoxy has been processed up to and including the soft-bake step described earlier. Next, the sample is subjected to final cure conditions to cure both materials.

Volume gratings can also be defined by laminating the photopolymer sheet prior to UV definition and exposing the sample through the fused-silica substrate upon which it resides. Figure 6 shows a plot of transmitted intensity versus incident angle for a slab (i.e., non-patterned) grating-within-the-waveguide volume grating that resides directly atop a fused-silica substrate (i.e., no intermediate epoxy layer). This grating exhibits approximately 72% input coupling efficiency at a near-normal angle of incidence, as indicated by the magnitude and location, respectively, of the dip in transmitted intensity.

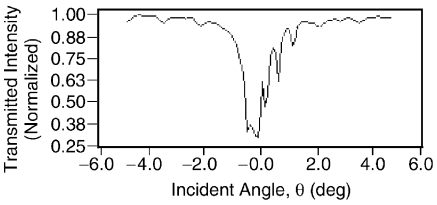

Figure 6. Transmitted intensity versus incident angle for grating-within-the-waveguide volume-grating coupler. The dip in the transmitted intensity curve indicates a Bragg angle of output/input coupling near 0°, while the ~72% dip in normalized intensity represents the input coupling efficiency.

Summary

The higher interconnect density and improved performance of integrated circuits have created a need for reducing the number of layers of packaging in microelectronic components. The introduction of compliant wafer-level packaging methods like the sea of leads can address the input/output needs of future integrated circuits. This approach can be used to facilitate the introduction of optical interconnects for integrated circuits.

References

1. J.D. Meindl, J.A. Davis, P. Zarkesh-Ha, C.S. Patel, K.P. Martin, and P.A. Kohl, *IBM J. Res. Dev.* **46** (2002) p. 245.
2. J.D. Meindl, R. Venkatesan, J.A. Davis, J. Joyner, A. Naeemi, P. Zarkesh-Ha, M.S. Bakir, A.V. Mulé, P.A. Kohl, and K.P. Martin, in *IEEE Int. Electron Devices Meet. Tech. Dig.* (Institute of Electrical and Electronics Engineers, Piscataway, NJ, 2001) p. 525.
3. *2001 International Technology Roadmap for Semiconductors* (ITRS) (Semiconductor Industry Association, San Jose, 2001).
4. M.S. Bakir, H.A. Reed, P.A. Kohl, K.P. Martin, and J.D. Meindl, in *Proc. IEEE Electronic Components and Technology Conf.* (Institute of Electrical and Electronics Engineers, Piscataway, NJ, 2002) p. 1087.
5. M.S. Bakir, H.A. Reed, A.V. Mulé, P.A. Kohl, K.P. Martin, and J.D. Meindl, in *Proc. Custom Integrated Circuits Conf.* (Institute of Electrical and Electronics Engineers, Piscataway, NJ, 2002) p. 491.
6. C.S. Patel, "Compliant Wafer-Level Package (CWLP)," PhD dissertation, Georgia Institute of Technology, 2001.
7. C.S. Patel, C. Power, M. Realff, P.A. Kohl, K.P. Martin, and J.D. Meindl, in *Proc. Int. Conf. on High-Density Interconnect and Systems Packaging* (International Microelectronics and Packaging Society, Washington, DC, and CMP Media, Manhasset, NY, 2000) p. 335.
8. H.D. Thacker, M.S. Bakir, D. Keezer, K.P. Martin, and J.D. Meindl, in *Proc. IEEE Electronic Components and Technology Conf.* (Institute of Electrical and Electronics Engineers, Piscataway, NJ, 2002) p. 1188.
9. H.A. Reed, C.E. White, V. Rao, S.A. Allen, C.L. Henderson, and P.A. Kohl, *J. Micromech. Microeng.* **11** (2001) p. 733.
10. X. Wu, H.A. Reed, L.F. Rhodes, E. Elce, R. Ravikiran, R.A. Shick, C.L. Henderson, S.A. Bidstrup Allen, and P.A. Kohl, *J. Electrochem. Soc.* **149** (10) (2002) p. S79.
11. X. Wu, H.A. Reed, L.F. Rhodes, E. Elce, R. Ravikiran, R.A. Shick, C.L. Henderson, S.A.

Allen, and P.A. Kohl, *J. Appl. Polym. Sci.* in press.
12. S.M. Schultz, E.N. Glytsis, and T.K. Gaylord, *Opt. Lett.* **24** (1999) p. 1708.
13. M. Jones, PhD thesis, Georgia Institute of Technology, 1995.
14. R. Villalaz, E.N. Glytsis, and T.K. Gaylord, *Appl. Opt.* **41** (2002) p. 5223.
15. A.V. Mulé, M. Bakir, J.P. Jayachandran, R. Villalaz, H. Reed, K. Martin, P. Kohl, E. Glytsis, T. Gaylord, J. Meindl, N. Agrawal, S. Ponoth, J. Plawsky, and P. Persans, in *Proc. IEEE Int. Interconnect Tech. Conf.* (Institute of Electrical and Electronics Engineers, Piscataway, NJ, 2002) p. 122.
16. A. Jain, S. Rogojevic, S. Ponoth, N. Agarwal, I. Matthew, W.N. Gill, P. Persans, M. Tomozawa, J.L. Plawsky, and E. Simonyi, *Thin Solid Films* **513** (2001) p. 398. □

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